

**CLAIM AMENDMENTS:**

Claim 1 (Currently Amended): A semiconductor apparatus comprising:

a substrate;

m electrically conductive layers formed on said substrate, m being an integer of 2 or more, potentials of said m electrically conductive layers being capable of being independently controlled; and

m semiconductor thin films, each including n at least one semiconductor devices, each semiconductor device including a second-conductive-type semiconductor layer so that there are n second-conductive-type semiconductor layers respectively, n being an integer of 2 or more, said m semiconductor thin films being bonded on surfaces of said m electrically conductive layers respectively in a one-to-one correspondence;

m common wiring lines disposed on said substrate, potentials of said m common wiring lines being capable of being independently controlled, said m common wiring lines being respectively electrically connected to said m electrically conductive layers in a one-to-one correspondence; and

n signal wiring lines disposed on said substrate, potentials of said n signal wiring lines being capable of being independently controlled;

wherein said n second-conductive-type semiconductor layers are disposed on each of said m electrically conductive layers and are electrically connected to said n signal wiring lines so that a k-th one of said n second-conductive-type semiconductor layers and a k-th one of said n signal wiring lines

are electrically connected in a one-to-one correspondence, k being an integer between 1 and n.

Claim 2 (Original): The semiconductor apparatus according to claim 1, further comprising an integrated circuit formed in said substrate, said substrate being a semiconductor substrate.

Claim 3 (Original): The semiconductor apparatus according to claim 1, further comprising an integrated circuit device disposed on said substrate, said substrate being an insulating substrate.

Claim 4 (Currently Amended): The semiconductor apparatus according to claim 1, wherein each said semiconductor device includes a first-conductive-type semiconductor layer and the a second-conductive-type semiconductor layer, a conductive-type of said second-conductive-type semiconductor layer being different from a conductive-type of said first-conductive-type semiconductor layer, and  
said first-conductive-type semiconductor layer being in contact with said electrically conductive layer.

Claim 5 (Canceled).

Claim 6 (Currently Amended): The semiconductor apparatus according to claim 1 ~~claim 5~~, wherein ends of said electrically conductive layers in a row direction of said semiconductor devices and ends of said semiconductor thin films in a row direction of said semiconductor devices are located on imaginary reference planes perpendicular to a surface of said substrate in such a way that said ends of said electrically conductive layers and said ends of said semiconductor thin films are in alignment.

Claims 7-10 (Canceled).

Claim 11 (Currently Amended): The semiconductor apparatus according to claim 1 ~~claim 10~~, further comprising individual interconnecting lines extending from upper surfaces of said second-conductive-type semiconductor layers of said semiconductor devices in said semiconductor thin films to said signal wiring lines.

Claim 12 (Original): The semiconductor apparatus according to claim 11, wherein said individual interconnecting lines are thin films formed by photolithography.

Claim 13 (Currently Amended): The semiconductor apparatus according to claim 2 ~~claim 10~~, wherein said integrated circuit includes a driving-IC for driving

said semiconductor devices, and said m common wiring lines and said n signal wiring lines are electrically connected to said driving-IC.

Claim 14 (Original): The semiconductor apparatus according to claim 1, wherein said semiconductor thin films mainly consist of compound semiconductor.

Claim 15 (Original): The semiconductor apparatus according to claim 1, wherein said semiconductor device is any of a light-emitting element, a light-sensing element, a Hall element, and a piezoelectric element.

Claim 16 (Original): The semiconductor apparatus according to claim 1, wherein said electrically conductive layers are made of any of metal and polysilicon.

Claim 17 (Withdrawn): An optical print head including the semiconductor apparatus of claim 1.

Claim 18 (Withdrawn): The optical print head of claim 17, wherein the semiconductor device in the first thin semiconductor film in the semiconductor apparatus is a light-emitting element, the semiconductor apparatus including a plurality of such light-emitting elements, the optical print head further including:  
a base for supporting the combined semiconductor apparatus;

a rod lens array for focusing the light emitted by the light-emitting elements in the combined semiconductor apparatus;  
a holder for holding the rod lens array; and  
at least one clamp for holding the base and the holder together.

Claim 19 (Withdrawn): An image-forming apparatus comprising at least one optical print head including the semiconductor apparatus of claim 1.

Claim 20 (Withdrawn): The image-forming apparatus of claim 19, further comprising:

a photosensitive drum selectively illuminated by the optical printing head to form a latent electrostatic image.

Claim 21 (Withdrawn): The image-forming apparatus of claim 20, further comprising:

a developing unit for supplying toner to develop the latent electrostatic image on the photosensitive drum; and

a transfer roller for transferring the developed image from the photosensitive drum to printing media.

Claim 22 (New): A semiconductor apparatus, comprising:

a substrate;

m electrically conductive layers formed on said substrate, m being an integer of 2 or more, potentials of said m electrically conductive layers being capable of being independently controlled;

m semiconductor thin films, each including n semiconductor devices, n being an integer of 2 or more, said m semiconductor thin films being bonded on surfaces of said m electrically conductive layers respectively in a one-to-one correspondence;

m common wiring lines disposed on said substrate, potentials of said m common wiring lines being capable of being independently controlled, said m common wiring lines being respectively electrically connected to said m electrically conductive layers in a one-to-one correspondence; and

n signal wiring lines disposed on said substrate, potentials of said n signal wiring lines being capable of being independently controlled;

wherein said n semiconductor devices are disposed on each of said m electrically conductive layers and are electrically connected to said n signal wiring lines so that a k-th one of said n semiconductor devices and a k-th one of said n signal wiring lines are electrically connected in a one-to-one correspondence, k being an integer between 1 and n.